ABSTRACT OF THE DISCLOSURE

A memory device is provided, which includes a data receive gate to buffer, in a first buffer, data to be inputted, a data transfer gate to input the data of the first buffer and buffer the same data in a second buffer, a data write gate to output the data of the second buffer to a data bus, and a memory cell to write and store the data in the data bus. In a control circuit thereof, data is not inputted to the first buffer by controlling the data receive gate and at the same time data is inputted to the second buffer by controlling the data transfer gate, depending on a time period from activation of a write enable signal to changing of a data mask signal.